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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/377,740 08/20/99 SHOJI

K 32014-150502

EXAMINER

MM41/0913

VENABLE
P O BOX
WASHINGTON DC 20043-9998

CRANE, S
ART UNIT PAPER NUMBER

2811
DATE MAILED:

09/13/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/377,740

Applicant(s)

SHOJI ET AL

Examiner

Sara W. Crane

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 June 2001 (CPA filing).
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 9-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 9-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 5-6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrews et al. and Tavana et al. in view of Kean. and Kawashima.

Andrews figure 4 shows a semiconductor integrated circuit, having functional blocks 408 and gate array blocks 412 and 402. These blocks are within an area which includes a center position of a semiconductor chip 400. Kean teaches that a field programmable gate array (such as Andrews block 412) has "basic cells" (column 13, line 33) arranged in lines (first sentence of abstract). Andrews teaches that 408 is an application specific block implemented using mask programmable-type logic (column 3, lines 45-48). The mask-programmable logic is programmed at the factory (column 1, lines 12-15). The Andrews I/O circuits 406, 416, 414 are placed in a second area surrounding the center area. The I/O circuits inherently "buffer" input and output signals, because these circuits separate the interior circuitry from the external circuitry. Kawashima provides a specific teaching of the buffering function of input/output circuitry. (See the abstract.) Andrews column 1, lines 17-21, teaches that the field programmable gate array can be programmed by the user (after receiving the device from the factory), and that re-programming can also be done. User programming and re-programming means that the user is "designing circuits for inclusion in the gate array block." Field programmable gate arrays are programmed by establishing electrical

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electrical connections between the cells of the array, a procedure that is discussed in detail in Kean. Tavana et al. also discusses field programming by routing electrical connections. See figure 3, block 20.

Claims 2-4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied to claims 1, 5-6 and 12 above, and further in view of Chan et al.

Chan et al. teaches at column 1, lines 26-28, that gate array, standard cell, full custom design, and programmable logic are alternative ways of designing specific integrated circuits. Any of these techniques would have been obvious, because each technique is known in the art, and therefore has known advantages, and because each of the techniques is an alternative to the others, as noted by Chan et al.

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied to claims 1, 5-6 and 12 above, and further in view of Dangelo.

Figure 2 of Dangelo teaches functional blocks that include CPU 102 and memory 108. It would have been obvious to include such blocks in the device of Andrews et al., in order to carry out the particular type of logic sequences associated with a CPU.

Conclusion

The arguments of 22 May 2001 have been considered, but are not convincing. Kean is relied upon to show the known structure of a field programmable

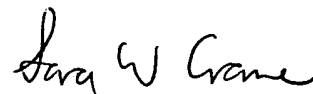
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gate array, and a field programmable gate array is taught by Andrews et al. If Applicant believes that the Kean teaching is not of a field programmable gate array, reasons should be provided. I/O buffers placed at the chip edges next to the pads are notoriously well-known, and both Kawashima and Andrews et al. show this feature specifically. The design difficulties involved with placement of I/O circuitry distant from the pads are clear upon a moments reflection. (One would have to run wiring from the pads to the I/O, of course.)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (703) 308-4894.

The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 308-0956.



Sara W. Crane
Primary Examiner
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